ABSTRACT

The ManArray core indirect VLIW processor consists of an array controller sequence processor (SP) merged with a processing element (PE0) closely coupling the SP with the PE array and providing the capability to share execution units between the SP and PE0. Consequently, in the merged SP/PE0 a single set of execution units are coupled with two independent register files. To make efficient use of the SP and PE resources, the ManArray architecture specifies a bit in the instruction format, the S/P-bit, to differentiate SP instructions from PE instructions. Multiple register contexts are obtained in the ManArray processor by controlling how the array S/P-bit in the ManArray instruction format is used in conjunction with a context switch bit (CSB) for the context selection of the PE register file or the SP register file. In arrays consisting of more than a single PE, the software controllable context switch mechanism is used to reconfigure the array to take advantage of the multiple context support the merged SP/PE provides. For example, a 1x1 can be configured as a 1x1 with context-0 and as a 1x0 with context-1, a 1x2 can be configured as a 1x2 with context-0 and as a 1x1 with context-1, and a 1x5 can be configured as a 1x5 with context-0 and as a 2x2 with context-1. Other array configurations are clearly possible using the present techniques. In the 1x5/2x2 case, the two contexts could be a 1x5 array (context-0) and a 2x2 array (context-1).